



XR28V382 / XR28V384

Evaluation Board

User Manual

Revision History

Document No.	Release Date	Change Description
1.0.0	1/27/14	Legacy Exar Manual
023UMR00	8/19/20	Corrected jumper number in Tables 11 and 12, corrected Tables 10 and 15.

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1.0 Introduction

This user's manual is for the XR28V382 and XR28V384 evaluation board. The XR28V384 is a 4-channel UART with Low Pin Count (LPC) bus interface in a 48-pin TQFP package. The XR28V382 is the 2-channel version available in a smaller 32-pin QFN package.

Table 1: Evaluation Board Ordering Part Numbers

Device Ordering Part Number	Evaluation Board Ordering Part Number	Device Package	Device Location
XR28V382IL32-F XR28V382IL32TR-F	XR28V382IL32-0A-EB	32-pin QFN	U2
XR28V384IM48-F XR28V384IM48TR-F	XR28V384IM48-0A-EB	48-pin TQFP	U3

2.0 Evaluation Board Overview

A block diagram of the evaluation board is shown in [Figure 1](#) below.

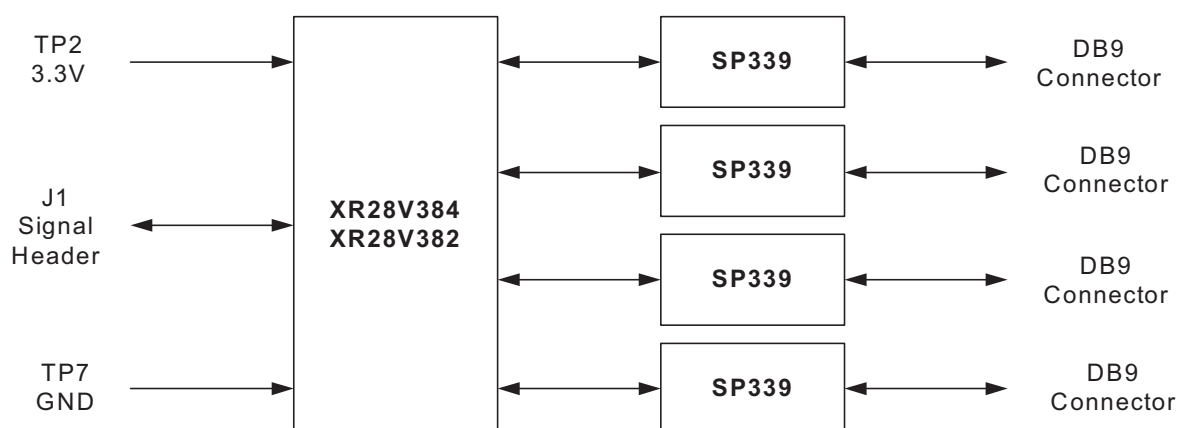


Figure 1: Evaluation Board Block Diagram

In addition to the XR28V384 or XR28V382, there is a MaxLinear SP339 Multiprotocol transceiver on this evaluation board. The SP339 can be configured for Loopback, RS-232, Half-Duplex RS-485 or Full-Duplex RS-485 / RS-422 Modes. The default setting when shipped from the factory is RS-232 mode.

[Figure 2](#) on the next page shows the top view of the evaluation board with all of the components, connectors and headers labeled.

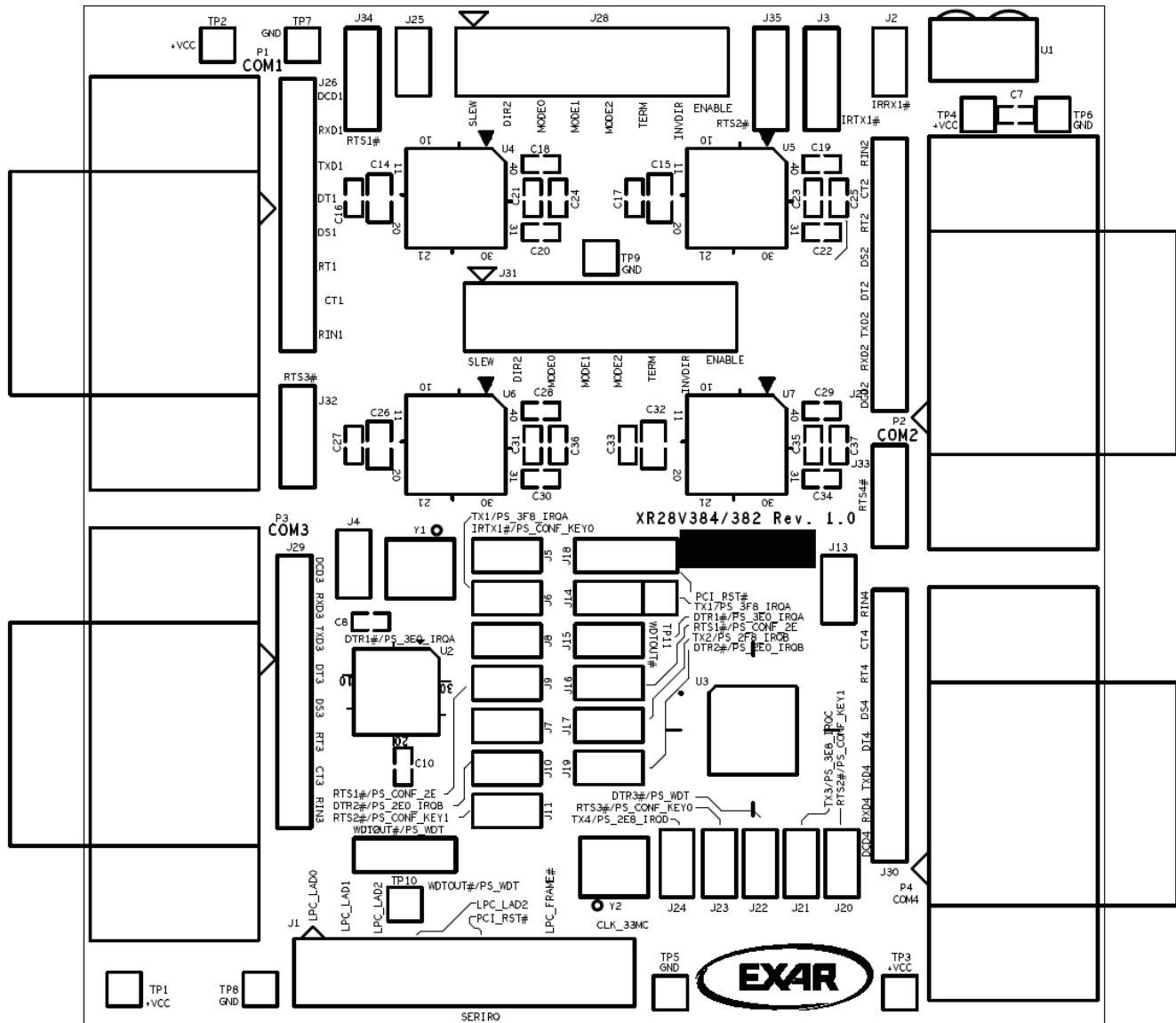


Figure 2: Top View of Evaluation Board

3.0 Hardware Configurations

This sections describes the default settings when shipped from the factory and what jumper setting changes are required when changing modes.

3.1 Power Requirements

External power is required for this board to function properly.

Table 2: Power Requirements

Test Point	Description
TP2	Apply an external +3.3V supply to this test point (or any other +3.3V test point).
TP7	Connect GND of external power supply to this test point (or any other GND test point).

3.2 LPC Bus Interface

All of the LPC interface signals are located on connector J1. These signals will need to be connected to an external LPC host controller. [Table 3](#) below provides a brief description of each signal.

Table 3: LPC Bus Interface Signals

Pin Number	Signal Name	Input / Output	Description
J1.1	LPC_LAD0	I/O	LPC Bus address / data bit-0
J1.3	LPC_LAD1	I/O	LPC Bus address / data bit-1
J1.5	LPC_LAD2	I/O	LPC Bus address / data bit-2
J1.7	LPC_LAD3	I/O	LPC Bus address / data bit-3
J1.11	PCI_RST#	Input	LPC Bus reset
J1.15	LPC_FRAME#	Input	LPC frame signal
J1.19	CLK_33MC	Input	33MHz PCI / LPC clock
J1.12	SERIRQ	Open-Drain Output	Serial IRQ

Refer to the datasheet for complete details and descriptions of each signal.

3.3 XR28V384 Configuration Jumper Settings

3.3.1 Reset

For normal operation, a jumper should be installed between J18.1 and J18.2. If a jumper is installed between J18.2 and J18.3, the XR28V384 will be in reset mode.

3.3.2 Configuration Port Selection

Table 4: Configuration Port Selection

Jumper (J16)	Index Port Address	Data Port Address
Yes	0x4E	0x4F
No	0x2E	0x2F

3.3.3 Configuration Entry Key Selection

Table 5: Configuration Entry Key Selection

Jumper1 (J20)	Jumper2 (J23)	Entry Key
Yes	Yes	0x77
Yes	No	0xA0
No	Yes	0x87
No	No	0x67

3.3.4 Base Address Selection

The XR28V384 has weak internal pull-up resistors for the configuration pins. On the evaluation board, there are pull-down resistors for selecting the base address and to enable / disable the different functions. "Yes" in the tables in the following sections indicate that the jumpers are installed.

3.3.4.1 UART Channel A Base Address Selection

Table 6: UART Channel A Base Address Selection

Jumper1 (J14)	Jumper2 (J15)	Base Address
No	No	0x3F8
No	Yes	0x3F8
Yes	No	0x3E0
Yes	Yes	0x000 (disabled)

3.3.4.2 UART Channel B Base Address Selection

Table 7: UART Channel B Base Address Selection

Jumper1 (J17)	Jumper2 (J19)	Base Address
No	No	0x2F8
No	Yes	0x2F8
Yes	No	0x2E0
Yes	Yes	0x000 (disabled)

3.3.4.3 UART Channel C Base Address

There are no selections for channel C. The channel C base address defaults to 0x3E8, if enabled. Channel C is enabled if there is no jumper installed on J21.

Table 8: UART Channel C Base Address

Jumper1 (J21)	Base Address
No	0x3E8
Yes	0x000 (disabled)

3.3.4.4 UART Channel D Base Address

There are no selections for channel D. The channel D base address defaults to 0x2E8, if enabled. Channel C is enabled if there is no jumper installed on J24.

Table 9: UART Channel D Base Address

Jumper1 (J24)	Base Address
No	0x2E8
Yes	0x000 (disabled)

3.3.4.5 Watchdog Timer Base Address

The watchdog timer base address defaults to 0x442. The watchdog timer is enabled if there is no jumper installed on J22.

Table 10: Watchdog Timer Base Address

Jumper1 (J22)	Base Address
No	0x442
Yes	0x000 (disabled)

Note: All base address registers can be overwritten after power-up. See the datasheet for details.

3.4 XR28V382 Configuration Jumper Settings

3.4.1 Reset

For normal operation, a jumper should be installed between J18.1 and J18.2. If a jumper is installed between J18.2 and J18.3, the XR28V382 will be in reset mode.

3.4.2 Configuration Port Selection

Table 11: Configuration Port Selection

Jumper (J9)	Index Port Address	Data Port Address
Yes	0x4E	0x4F
No	0x2E	0x2F

3.4.3 Configuration Entry Key Selection

Table 12: Configuration Entry Key Selection

Jumper1 (J11)	Jumper2 (J5)	Entry Key
Yes	Yes	0x77
Yes	No	0xA0
No	Yes	0x87
No	No	0x67

3.4.4 Base Address Selection

The XR28V382 has weak internal pull-up resistors for the configuration pins. On the evaluation board, there are pull-down resistors for selecting the base address and to enable / disable the different functions. "Yes" in the tables in the following sections indicate that the jumpers are installed.

3.4.4.1 UART Channel A Base Address Selection

Table 13: UART Channel A Base Address Selection

Jumper1 (J6)	Jumper2 (J8)	Base Address
No	No	0x3F8
No	Yes	0x3F8
Yes	No	0x3E0
Yes	Yes	0x000 (disabled)

3.4.4.2 UART Channel B Base Address Selection

Table 14: UART Channel B Base Address Selection

Jumper1 (J7)	Jumper2 (J10)	Base Address
No	No	0x2F8
No	Yes	0x2F8
Yes	No	0x2E0
Yes	Yes	0x000 (disabled)

3.4.4.3 Watchdog Timer Base Address

The watchdog timer base address defaults to 0x442. The watchdog timer is enabled if there is no jumper installed on J22.

Table 15: Watchdog Timer Base Address

Jumper1 (J12)	Base Address
Pins 1 & 2	0x442
Pins 2 & 3	0x000 (disabled)

4.0 Software

4.1 BIOS Support

The BIOS needs to have support for detecting and / or configuring devices on the LPC bus. If the BIOS does not support this function and this function is not added to the BIOS, then the operating system may not be able to access some or all of these ports.

4.2 Software Drivers

The XR28V384 and XR28V382 are software compatible with the industry standard 16550 UARTs. Hence, they will work with any OS that has a standard serial port drivers such as Windows and Linux.



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